What is claimed is:

1. A semiconductor memory device comprising:

a plurality of memory cell arrays, each of which includes a plurality of memory cells;

a plurality of redundant judgment circuits, each of which is used for storing an address of a defective memory cell of the corresponding memory cell array, wherein each of the redundant judgment circuits include a block judgment unit which outputs a block judgment signal and an address judgment unit which outputs a redundant judgment signal; and

a redundant memory cell array,

wherein the block judgment unit outputs the block judgment signal when the corresponding memory cell array includes the defective memory cell, and

wherein the address judgment unit outputs the redundant judgment signal when the block judgment signal is output from the block judgment unit and the address of the defective memory cell matches an external address, so that the redundant memory cell array is accessed in place of the corresponding memory cell array which includes the defective memory cell.

2. The semiconductor memory device of claim 1, wherein the block judgment unit includes a fuse.

3. The semiconductor memory device of claim 2, wherein each of the block judgment units including a latching circuit which latches a level of the block judgment signal in response to a connection state of the fuse.

4. The semiconductor memory device of claim 1, wherein the address judgment unit includes a fuse, and wherein the address judgment unit judges the address of the defective memory cell in response to a connection of state of the fuse.

5. The semiconductor memory device of claim 1, wherein the address judgment unit comprises a comparing circuit which includes a plurality of comparing gates, wherein the external address and the address of the defective memory cell are compared at every bit in the respective comparing gate.

6. A semiconductor memory device comprising:

a plurality of memory cell arrays, each of which includes a plurality of memory cells;

a plurality of redundant judgment circuits, each of which is used for storing an address of a defective memory cell of the corresponding memory cell array, wherein each of the redundant judgment circuits include a block judgment unit which outputs a block judgment signal and an address judgment unit which outputs a redundant judgment signal; and

a redundant memory cell array,

wherein the block judgment unit outputs the block judgment signal when the corresponding memory cell array is selected and the corresponding memory cell array includes the defective memory cell, and

wherein address judgment unit outputs the redundant judgment signal when the address of the defective memory cell matches an external address, so that the redundant memory cell array is accessed in place of the corresponding memory cell array which includes the defective memory cell.

7. The semiconductor memory device of claim 6, wherein the block judgment unit includes a fuse.

8. The semiconductor memory device of claim 7, wherein each of the block judgment unit including a latching circuit which latches a level of the block judgment signal in response to a connection state of the fuse.

9. The semiconductor memory device of claim 6, wherein the address judgment unit includes a fuse, and wherein the address judgment unit judges the address of the defective memory cell in response to a connection of state of the fuse.

10. The semiconductor memory device of claim 6, wherein the address judgment unit comprises a comparing circuit which includes a plurality of comparing gates, wherein the external address and the address of the defective memory cell are compared at every bit

in the respective comparing gate.